generating a first output signal having a first state in accordance with the input signal using the first drive circuit; and

driving the second drive circuit to generate a second output signal having the first state by a driving signal which is generated by adding a predetermined delay to the output signal.

2. (Thrice Amended) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor connected between a first power supply and an output terminal of the output buffer circuit and a second output transistor connected between a second power supply and the output terminal, the second drive circuit including a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal using the first drive circuit;

generating a delay signal by delaying the output signal;

generating a control signal for controlling the third and fourth output transistors in accordance with the delay signal and the input signal; and

driving the second drive circuit to generate a second output signal having the first state by the control signal.

5. (Thrice Amended) An output buffer circuit comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first output signal having a first state;

a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit, wherein the second drive circuit generates a second output signal; and

C3 cont. a first control circuit, connected to the second drive circuit, for generating a first control signal for driving the second drive circuit on the basis of the input signal and a delay signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates the second output signal having the first state.

23. (Amended) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor of a first type and a second output transistor of a second type, the second drive circuit C4 including a third output transistor of the first type and a fourth output transistor of the second type, the third and fourth output transistors having lower impedances than the first and second output transistors, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal by turning on the first transistor of the first drive circuit; and

driving the second drive circuit to generate a second output signal having the first state by turning on the third transistor of the second drive circuit by a driving signal which is generated by adding a predetermined delay to the first output signal.

C5 25. (Amended) An output buffer circuit comprising:

a first drive circuit including a first transistor of a first type and a second output transistor of a second type which are connected to an output terminal, wherein the first and second transistors receive an input signal and generate a first output signal having a first state by turning on the first transistor or the second transistor;

a second drive circuit including a third transistor of the first type and a fourth transistor of the second type which are connected to the output terminal, wherein the third and fourth output transistors have lower impedances than the first and second output transistors; and

C5 Com.

a first control circuit, connected to the second drive circuit, for generating a first control signal for turning on the third transistor on the basis of the input signal and a delay signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates a second output signal having the first state.

A marked-up copy of the amended claims is attached as required under 37 C.F.R. § 1.121.

Please add new claims 28 and 29 as follows:

Cb

28. (New) A method of controlling an output buffer circuit for generating an output signal and outputting the output signal from an output terminal, wherein the output buffer circuit includes a first drive circuit for receiving an input signal, and a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal using the first drive circuit;

monitoring whether the first output signal is changed by a predetermined amount; and

driving the second drive circuit to generate a second output signal having the first state when monitoring that the first output signal is changed by a predetermined amount.

29. (New) An output buffer circuit comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first output signal having a first state;

a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit for generating a second output signal; and

a first control circuit connected to the second drive circuit for monitoring whether the first output signal is changed by a predetermined amount and generating a first control signal when monitoring that the first output signal is changed by a predetermined amount, wherein the first control signal drives the second drive circuit such that the second drive circuit generates the second output signal having the first state.

REMARKS

The following remarks are fully and completely responsive to the Office Action dated November 1, 2002. Claims 1-11 and 19-29 are pending in this application with claims 28 and 29 added by the present Amendment. In the outstanding Office Action, claim 23 was objected to and claims 1-11 and 19-27 were rejected under 35 U.S.C. §